1.0 Overview

The OPTi 82C621A PCI IDE Controller (PIC) is a 100-pin controller chip designed for a fast and flexible interface between the PCI bus and two IDE cables. The 82C621A implements a PCI function to directly support both the Primary and Secondary IDE in a single 100-pin PQFP. This high-integration approach reduces component count, eases board design, reduces cost and increases reliability. An integrated 4-level read-prefetch FIFO and a 4-level posted write FIFO supports zero wait-state operations, substantially improving performance over other IDE implementations. The Enhanced ATA Specification can be supported either by setting Strap Options or by programming internal registers.

2.0 Features

- Supports 32-bit PCI Bus & Configuration Registers
- 100-pin PQFP
- Supports 4 ATA peripherals
- Optional PCI Expansion ROM support
- 16-byte Read-Prefetch and Write-Posting FIFO
- IDE timing controlled by either Straps or Registers
- Programming interface compatible with 82C611A

2.1 Special Feature Notes

Write Posting and Read-prefetch allows CPU memory cycles to run concurrently with IDE cycles and also removes the synchronization penalty for AT-bus transfers. IDE cycles can be fine tuned by the ANSI Mode strap options or programmable registers for ANSI-standard (mode 0, 1, 2 or 3) devices or non-standard devices. 32-bit PCI cycles translated to two 16-bit IDE cycles for faster data access.

Figure 2-1 Block Diagram

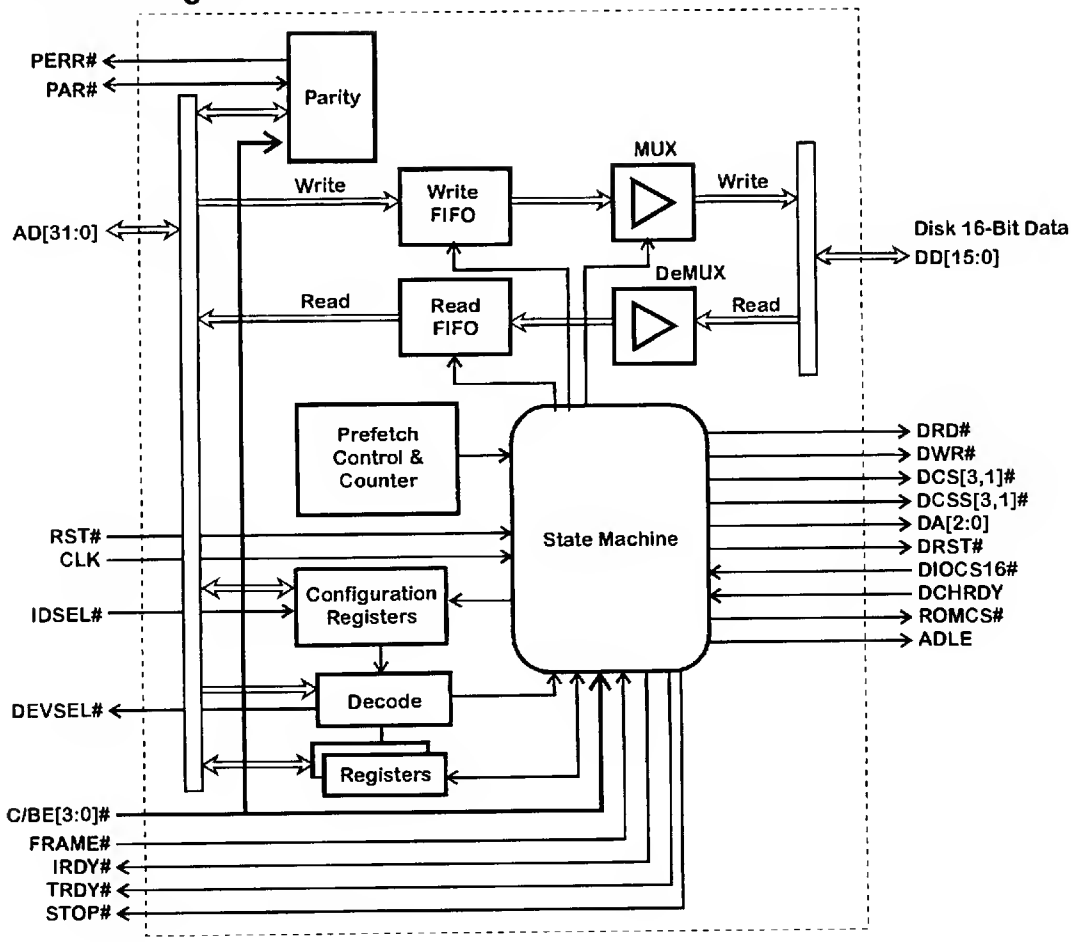
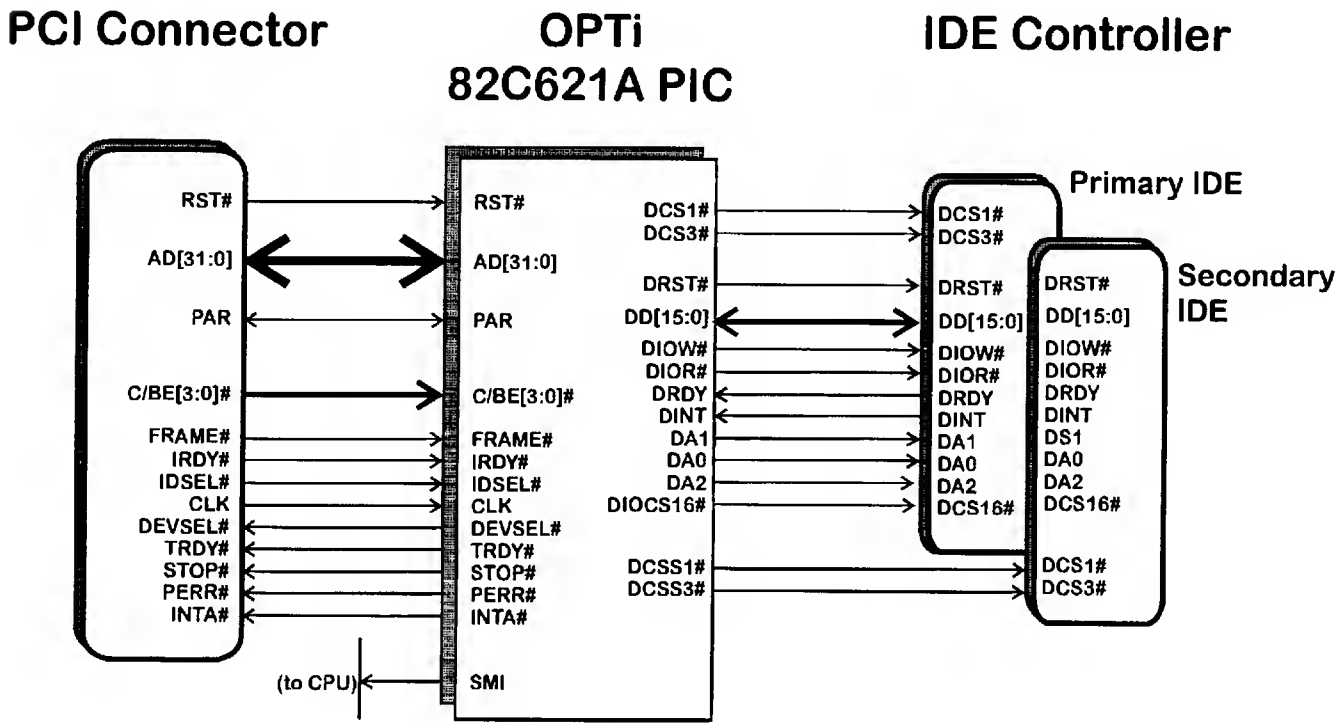


Figure 2-2 Example PCI Controller Block Diagram



3.0 Signal Description

Figure 3-1 Pin Diagram

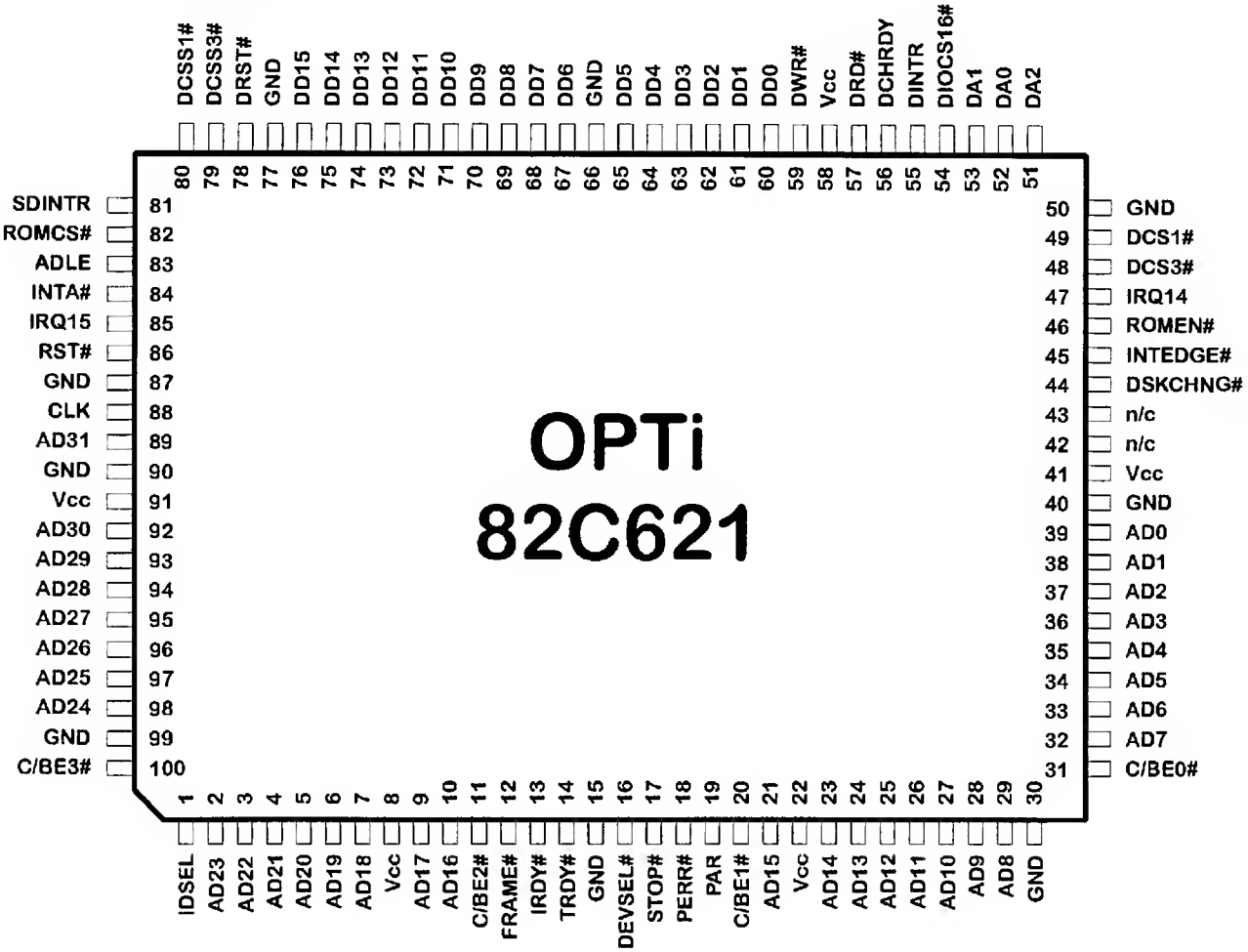


Table 3-1 Numerical Pin List

Name	Pin	Name	Pin	Name	Pin	Name	Pin
IDSEL	1	AD11	26	DA2	51	DD15	76
AD23	2	AD10	27	DA0	52	GND	77
AD22	3	AD9	28	DA1	53	DRST#	78
AD21	4	AD8	29	DIOCS16#	54	DCSS3#	79
AD20	5	GND	30	DINTR	55	DCSS1#	80
AD19	6	C/BE0#	31	DCHRDY	56	SDINTR#	81
AD18	7	AD7	32	DRD#	57	ROMCS#	82
VCC	8	AD6	33	VCC	58	ADLE	83
AD17	9	AD5	34	DWR#	59	INTA#	84
AD16	10	AD4	35	DD0	60	IRQ15	85
C/BE2#	11	AD3	36	DD1	61	RST#	86
FRAME#	12	AD2	37	DD2	62	GND	87
IRDY#	13	AD1	38	DD3	63	CLK	88
TRDY#	14	AD0	39	DD4	64	AD31	89
GND	15	GND	40	DD5	65	GND	90
DEVSEL#	16	VCC	41	GND	66	VCC	91
STOP#	17	n/c	42	DD6	67	AD30	92
PERR#	18	n/c	43	DD7	68	AD29	93
PAR	19	DSKCHNG#	44	DD8	69	AD28	94
C/BE1#	20	INTEDGE#	45	DD9	70	AD27	95
AD15	21	ROMEN#	46	DD10	71	AD26	96
VCC	22	IRQ14	47	DD11	72	AD25	97
AD14	23	DCS3#	48	DD12	73	AD24	98
AD13	24	DCS1#	49	DD13	74	GND	99
AD12	25	GND	50	DD14	75	C/BE3#	100

Table 3-2 Alphabetical Pin List

Name	Pin
AD0	39
AD1	38
AD2	37
AD3	36
AD4	35
AD5	34
AD6	33
AD7	32
AD8	29
AD9	28
AD10	27
AD11	26
AD12	25
AD13	24
AD14	23
AD15	21
AD16	10
AD17	9
AD18	7
AD19	6
AD20	5
AD21	4
AD22	3
AD23	2
AD24	98

Name	Pin
AD25	97
AD26	96
AD27	95
AD28	94
AD29	93
AD30	92
AD31	89
ADLE	83
C/BE0#	31
C/BE1#	20
C/BE2#	11
C/BE3#	100
CLK	88
DA0	52
DA1	53
DA2	51
DCHRDY	56
DCS1#	49
DCS3#	48
DCSS1#	80
DCSS3#	79
DD0	60
DD1	61
DD2	62
DD3	63

Name	Pin
DD4	64
DD5	65
DD6	67
DD7	68
DD8	69
DD9	70
DD10	71
DD11	72
DD12	73
DD13	74
DD14	75
DD15	76
DEVSEL#	16
DINTR	55
DIOCS16#	54
DRD#	57
DRST#	78
DSKCHNG#	44
DWR#	59
FRAME#	12
GND	15
GND	30
GND	40
GND	50
GND	66

Name	Pin
GND	77
GND	87
GND	90
GND	99
IDSEL	1
INTA#	84
INTEDGE#	45
IRDY#	13
IRQ14	47
IRQ15	85
n/c	42
n/c	43
PAR	19
PERR#	18
ROMCS#	82
ROMEN#	46
RST#	86
SDINTR#	81
STOP#	17
TRDY#	14
VCC	8
VCC	22
VCC	41
VCC	58
VCC	91

3.1 Pin Assignments

3.1.1 PCI-BUS Interface

Name	Type	Pin	Description
AD[31:0]	I/O	89, 92-98, 2-7, 9,10,21, 23-29, 32-39	***Address/Data.*** Multiplexed address/data lines of the PCI bus. A bus transaction includes an address phase followed by one or more data phases.
C/BE[3:0]#	I	100,11,20,31	***Bus Command/Byte Enable.*** These lines define the bus command during the address phase of a bus transaction. During the data phase, these lines define the byte enables.
CLK	I	88	***PCI Bus Clock.*** This signal provides timing for all PCI transactions.
DEVSEL#	O	16	***Device Select.*** This output indicates that the current address on the PCI-bus is addressing the PIC.
FRAME#	I	12	***Cycle Frame.*** This signal is asserted to indicate a bus transaction is beginning and de-asserted at the end of the address phase.
IDSEL	I	1	***Initialization Device Select.*** This is used as a chip select during configuration read/write cycles.
INTA#/IRQ14	O	84	***Interrupt A/Interrupt Request 14.*** When pin 79 (DCSS3#) is high at reset, this is used as IRQ14. When pin 79 is low at reset, the pin is used as INTA#. Refer to Section 3.2, Oldmode vs. Newmode for more information.
IRDY#	I	13	***Initiator Ready.*** This signal indicates the bus masters ability to complete the current data phase.
IRQ15	O	85	***Interrupt Request 15.*** This is used as IRQ15. Refer to Section 3.2, Oldmode vs. Newmode for more information.
PAR	I/O	19	***Parity.*** This signal indicates even parity across AD[31:0] and C/BE[3:0]#.
PERR#	O	18	***Parity Error.*** This signal is used to report data parity errors.
RST#	I	86	***Reset.*** This signal is used to initialize the PIC and any drives attached.
STOP#	O	17	***Stop.*** This signal indicates that the target is requesting the master to stop the current transaction.
TRDY#	O	14	***Target Ready.*** This signal indicates the targets ability to complete the current data phase of the transaction.

3.1.2 IDE Interface

Name	Type	Pin	Description
DA[1:0] / MODE[1:0]	I/O	53,52	***Drive Address Lines/Mode [1:0].*** These are the two lower bits of the 3-bit binary coded address asserted by the host to access a register or data port in the drive. At reset time, Mode [1,0] are sampled to set the IDE Device Modes for 16-bit Cycle Times: Mode 1 Mode 0 Cycle-Time 0 0 ≥ 600ns 0 1 ≥ 383ns 1 0 ≥ 240ns 1 1 ≥ 180ns These pins are also used to enter one of four test modes if TMOD# is sampled low at reset: Mode 1 Mode 0 Test Mode 0 0 Tri-state all output and bi-directional signals, 0 1 Output of input & bi-directional NAND chain on Pin 42 (all bi-directional signals tri-stated), 1 0 Drive all even pin outputs high and odd low, 1 1 Drive all odd pin outs high and even low
DA2/ENPREF	I/O	51	***Drive Address Line 2/Enable Prefetch.*** This is the MSB of the 3-bit binary coded address asserted by the host to access a register or data port in the drive. At reset time, *ENPREF* is sampled to set the Miscellaneous Register bit 6 which decides whether to enable or disable read prefetch. 1 = Enable, 0 = Disable
DCHRDY	I	56	***I/O Channel Ready.*** This signal is negated to extend the host transfer cycle of any host register access (Read or Write) when the drive is not ready to respond to a data transfer request. When DCHRDY is not negated, DCHRDY is in a high impedance state.
DCS1# / SPD0	I/O	49	***Drive Chip Select 1.*** This is the chip select signal decoded from the host address bus used to select the Command Block Registers for the primary IDE. At reset time, *SPD0* is sampled to set the Strap Register bit 0 (PCI-bus frequency select, LSB), which determines the exact PCI-bus frequency: SPD0 Frequency 0 33 MHz 1 25 MHz
DCS3# / PCI3F7	I/O	48	***Drive Chip Select 3.*** This is the chip select signal decoded from the host address bus used to select the Control Block Registers for the primary IDE. At reset time, *PCI3F7* is sampled to set the Strap Register bit 7, which decides whether or not to respond to I/O port 3F7h from the local bus. 0 = 3F7h read from local bus, 1 = No response to 3F7h read

3.1.2 IDE Interface (cont.)

Name	Type	Pin	Description
DCSS1# / RELOC	I/O	80	***Secondary Drive Chip Select 1.*** This is the chip select signal decoded from the host address bus used to select the Command Block Registers for the secondary IDE. At reset time, RELOC is sampled to decide whether the I/O space addresses are relocatable through programming configuration space registers. 0 = Fixed I/O addresses (1F0h-1F7h, 3F6h for primary; 170h-177h, 376h for secondary). 1 = Relocatable I/O addresses.
DCSS3#/ INTMODE	O	79	***Secondary Drive Chip Select 3.*** This chip select signal is decoded from the host address bus used to select the Control Block Registers for the secondary IDE. *Interrupt Mode.* When pin 79 is high during reset, the INTA# and IRQ15 interrupt functions remain the same (oldmode). When pin 79 is low during reset, a different definition for the interrupt pins (84 and 85) is set (newmode). Refer to section 3.2 oldmode vs. newmode for more information.
DD[15:0]	I/O	76-67, 65-60	***Disk Data Bus Lines 0 to 15.*** These sixteen data bus lines require an external pull-up.
DIOCS16#	I	54	***Drive 16-bit I/O.*** DIOCS16# indicates that the 16-bit data port has been addressed and that the drive is prepared to send or receive a 16-bit data word. If DIOCS16# is not asserted, transfers are 8-bit using DD[7:0]. If DIOCS16# is asserted, transfers are 16-bit using DD[15:0].
DRD#	O	57	***Drive I/O read.*** This is the Read strobe signal. The low level of DRD# enables data from a register or the data port of the drive onto the data bus DD[7:0] or DD[15:0].
DWR#	O	59	***Drive I/O write.*** This is the Write strobe signal. The rising edge of DWR# samples data from the data bus DD[7:0] or DD[15:0] into a register or the data port of the drive.
DINTR	I	55	***Drive interrupt.*** This signal is used to interrupt the host system for the primary IDE. DINTR is asserted only when the drive has a pending interrupt, the drive is selected, and the host has cleared nIEN in the Device Control Register. DINTR is negated by assertion of DRST#, the setting of SRST of the Device Control Register, the host writing the Command Register, or the host reading the Status Register DINTR is asserted at the beginning of each data block to be transferred. A data block is typically a single sector, except when declared otherwise by use of the Set Multiple command. An exception to this occurs on Format Track, Write Sector(s), Write Buffer and Write Long commands where DINTR is not asserted at the beginning of the first data block to be transferred.
DRST#	O	78	***Drive reset.*** This signal is asserted for at least 25 µsec after voltage levels have stabilized during power on and negated thereafter unless some event requires that the drive(s) be reset following power on.

3.1.2 IDE Interface (cont.)

Name	Type	Pin	Description
SDINTR	I	81	***Secondary Drive interrupt.*** This signal is used to interrupt the host system for the secondary IDE. SDINTR is asserted only when the drive has a pending interrupt, the drive is selected, and the host has cleared nIEN in the Device Control Register. SDINTR is negated by assertion of DRST#, the setting of SRST of the Device Control Register, the host writing the Command Register, or the host reading the Status Register SDINTR is asserted at the beginning of each data block to be transferred. A data block is typically a single sector, except when declared otherwise by use of the Set Multiple command. An exception to this occurs on Format Track, Write Sector(s), Write Buffer and Write Long commands where DINTR is not asserted at the beginning of the first data block to be transferred.

3.1.3 AT-Bus Interface

Name	Type	Pin	Description
DSKCHNG#	I	44	***Disk-Change-Line.*** For configurations including a floppy controller, this signal can be connected to the drive-change line.

3.1.4 ROM Support/Power Management Interface

Name	Type	Pin	Description
ADLE/FNC0	I/O	83	***Address Latch Enable/Function 0.*** ADLE output is used to latch ROM addresses 0 through 7 when ROM is enabled. At reset time, Function 0 is sampled to enable different functions of the chip, as follows: FNC0 Function 0 Both Primary and Secondary IDE enabled 1 Primary IDE only
ROMEN#	I	46	***ROM Enable.*** At reset time, this pin is sampled to enable or disable expansion ROM. 0 = Enable. 1 = Disable.
ROMCS#/ SMI#/ TMOD#	I/O	82	***ROM Chip Select/System Management Interrupt/Test Mode.*** ROM Chip Select is used to enable the ROM output and ROM data buffer. SMI# is used to signal to the host system that an SMI event has occurred. The function of this pin is determined by the sampling of ROMEN# strap option. At reset time, TMOD# is sampled to enable test mode. This line requires an external pull up, and must be sampled high at the end of reset for normal operation. 0 = Test mode. 1 = User mode.

3.1.5 Miscellaneous Pins

Name	Type	Pin	Description
IRQ14	O	47	***Interrupt Request 14.*** This pin is normally used as IRQ14 when pin 79 is high at reset. Refer to Section 3.2, Oldmode vs. Newmode for more information on this function.

3.1.5 Miscellaneous Pins (cont.)

Name	Type	Pin	Description
INTEDGE#	I	45	***Interrupt Level/Edge.*** When pin 79 is high at reset, this pin is sampled to decide whether INTA# and IRQ15 are edge or level triggered interrupts. 0 = Edge triggered (Active high). 1 = Shared level triggered (Active low). When pin 79 is low at reset, the strap function is disabled.

3.1.6 Power and Ground Pins

Name	Type	Pin	Description
GND	I	15,30,40,50,66,77,87,90,99	Vss or Ground
VCC	I	8,22,41,58,91	Vcc or +5v

3.2 Oldmode vs. Newmode

A new strap option has been added to pin 79 (DCSS3#) to select the mode that the 82C621A will run in. The features that are affected by this strap are:

1. When pin 79 is high during reset, the INTA# and IRQ15 interrupt functions remain the same. This is called oldmode. When pin 79 is low during reset, a different definition for the interrupt pins (84 and 85) is given in the table below. This is called newmode. Pin 79 is pulled high internally.
2. Interrupt pins 84 and 85, and pin 47 are renamed and redefined based on the newmode strap option.

The new names are:

Pin	Name
84	INTA#
85	IRQ15
47	IRQ14

The new definitions are:

Actual mode of operation*	Interrupt level Strap	Pin (oldmode)			Pin (newmode)		
		84	85	47	84	85	47
Legacy	Edge	14	15	14	3st†	15	14
Legacy	Level	14#‡	15#	14	3st	15	14
Native	Edge	14	15	3st	INTA#	3st	3st
Native	Level	14#	15#	3st	INTA#	3st	3st

* Refer to Section Section 4.6, Class Code Register (09h, R/W), bits 7:0 for information on setting Legacy and Native modes.

† 3st = Tri-state

‡ # = active low

Note Oldmode is only for compatibility with older versions of the 82C621. All new designs should use newmode for software compatibility with other vendor's devices.

4.0 Configuration Register Descriptions

This section describes the registers implemented in the 256 byte configuration space. All registers not implemented always return zero during read cycles.

Optionally, the PIC will support an expansion ROM on the PCI IDE plug-in board. This support will require two extra TTLs, as address latch and data buffer, on board. Also this will require a 32 bit register in the configuration space that normally would not be enabled. The expansion ROM base address register (offset 30h-33h) will be enabled only if the ROMEN# strap pin is sampled low at the time of reset.

4.1 Vendor ID Register (00h, Read Only)

Bits	Mnemonic	Description	Default
15:0	VID	***Vendor ID:*** This register identifies the OPTi ID.	1045h

4.2 Device ID Register (02h, Read Only)

Bits	Mnemonic	Description	Default
15:0	DID	***Device ID:*** This register identifies the ID of the PIC.	C621h

4.3 Command Register (04h, R/W)

Bits	Mnemonic	Description	Default
[15:7]	----	Reserved - Read only.	0
6	PEN	***Parity Checking Enable:*** When this bit is set, PIC generates PERR# if a parity error occurs during I/O write cycles. If the bit is reset, parity checking is ignored. For I/O read cycles, PIC always generates the parity bit.	0
[5:2]	----	Reserved - Read only.	0
1	MEMEN	***Memory Enable:*** When this bit is set and the expansion ROM enable bit is set (in the EPROM Register), the ROM space becomes available for reading.	0
0	IOEN	***Input/Output Enable:*** When this bit is set, PIC enables the I/O accesses. If reset, all I/O accesses are disabled.	1

4.4 Status Register (06h, R/W)

Bits	Mnemonic	Description	Default
15	PER	***Parity Error:*** This bit is set whenever the PIC detects a parity error. This bit is cleared by writing 8000h to this register.	0
[14:11]	----	Reserved - Read Only.	0
[10:9]	SELTIM	***Select Timing:*** These are read only bits indicating allowable timing assertion for DEVSEL#.	01
8	-----	Reserved - Read only.	0
7	BTB	***Back-To-Back Transactions.*** This is a read only bit, set to 1 to allow fast back-to-back transactions.	1
[6:0]	-----	Reserved - Read only.	0

4.5 Revision ID Register (08h, Read Only)

Bits	Mnemonic	Description	Default
7:0	REVID	***Revision ID:*** This register identifies the revision number of the PIC.	0

4.6 Class Code Register (09h, R/W)

Bits	Mnemonic	Description	Default
23:8	CCODE (read only)	***Class Code:*** The MSB indicates the base class code for the mass storage controller. The middle byte indicates the sub class code (IDE controller).	0101h
7:0	PI	***Programming Interface.*** When this register is defined as read/write, the first byte is used to define the IDE as relocatable (native mode) or fixed (legacy mode). Bits 0 and 1 are used for the primary IDE and bits 2 and 3 are used for the secondary IDE. Bits 0 and 2 show whether the IDE is in native mode or legacy mode and bits 1 and 3 show the setting of the RELOC strap option (0=low, 1=high). Bits 4 through 7 are reserved and set to 0. If the RELOC strap is low during reset, the IDE configuration is fixed (no relocatable) and the PI register bits are set to 0. If the RELOC strap is high during reset, the configuration space is definable and the PI register is accessible: bits 1 and 3 are set to 1 and bits 0 and 2 are used to define the IDE mode. Also, if the FNC0 strap is set to support the primary IDE only, bits 2 and 3 will not be used.	

4.7 Header Type Register (0Eh, Read Only)

Bits	Mnemonic	Description	Default
7:0	HDR	***Header Type:*** Single function device.	00h

4.8 Command Block Base Address Register (10h, R/W) (Primary IDE)

Bits	Mnemonic	Description	Default
31:0	IO1	***Command Block Base Address:*** This register is the I/O space indicator for the Drive Command Block. The address block has a size of 8 bytes. Bit [2:0] of this register are read only and default to 001. Bits [31:3] are writable if RELOC strap is set to 1. If the RELOC strap is set to 0, bits [31:0] are read only and return 0.	1F1h w/ RELOC=1

4.9 Control Block Base Address Register (14h, R/W) (Primary IDE)

Bits	Mnemonic	Description	Default
31:0	IO2	***Control Block Base Address:*** This register is the I/O space indicator for the Drive Control Block. The address block has a size of 4 bytes. Bit [1:0] of this register are read only and default to 01. Bits [31:2] are writable if RELOC strap is set to 1. If the RELOC strap is set to 0, bits [31:0] are read only and return 0.	3F5h w/ RELOC=1

4.10 Command Block Base Address Register (18h, R/W) (Secondary IDE)

Bits	Mnemonic	Description	Default
31:0	IO3	***Command Block Base Address:*** This register is the I/O space indicator for the Drive Command Block. The address block has a size of 8 bytes. Bit [2:0] of this register are read only and default to 001. Bits [31:3] are writable if RELOC strap is set to 1. If the RELOC strap is set to 0, bits [31:0] are read only and return 0.	171h w/ RELOC=1 FNC0=0

4.11 Control Block Base Address Register (1Ch, R/W) (Secondary IDE)

Bits	Mnemonic	Description	Default
31:0	IO4	***Control Block Base Address:*** This register is the I/O space indicator for the Drive Control Block. The address block has a size of 4 bytes. Bit [1:0] of this register are read only and default to 01. Bits [31:2] are writable if RELOC strap is set to 1. If the RELOC strap is set to 0, bits [31:0] are read only and return 0.	375h w/ RELOC=1 FNC0=0

4.12 External ROM Base Address Register (30h, R/W)

Bits	Mnemonic	Description	Default
31:0	EROM	***External ROM Base Address:*** This register contains the expansion ROM address. The address block has a size of 16KB. Bits [13:1] of this register are always read only and default to 0. Bits [31:14, 0] are writable if the ROMEN# strap is sampled low. Bits [31:14] define the base address of the expansion ROM. Bit 0 enables/disables the expansion ROM decode (0 = disable, 1 = enable). If the ROMEN# strap is sampled high, this register is read only (always 0) and ROM decode is disabled.	x

4.13 Interrupt Line Register (3Ch, R/W)

Bits	Mnemonic	Description	Default
7:0	INTL	***Interrupt Line.*** This register indicates which input of the system interrupt controller the INTA# interrupt pin is routed to.	Eh

4.14 Interrupt Pin Register (3Dh, Read Only)

Bits	Mnemonic	Description	Default
7:0	INTP	***Interrupt Pin.*** The content of this register is 1 (i.e., INTA# will be used).	1

5.0 I/O Register Descriptions

5.1 I/O Registers for Primary IDE

The register addresses are referred to in this section by their power-up default addresses. If the power-up default is modified by writing to configuration register IO1, then these registers will be relocated accordingly.

The PIC contains registers at seven I/O ports accessible after two consecutive 16-bit I/O reads from address 1F1h. Any other
I/O cycle between these two reads will disable access to the PIC registers.

5.1.1 Internal ID Register (1F2h, Write Only)

Bits	Mnemonic	Description	Default
7	CNFDIS	***Configuration Disable:*** This bit must be set to '0' in order to access 621A Internal Registers. Any write to this register with CNFDIS = 1 will disable all accesses to the 621A registers until another two consecutive I/O reads from 1F1h.	1
6	CNFOFF	***Configuration Off.*** This bit must be set to '0' in order to access 621A Internal Registers. Any write to this register with CNFOFF = 1 will disable all accesses to the 621A registers until power down or reset.	0
[5:2]	----	Reserved - Must be written 0.	
[1:0]	----	Reserved - Must be written 11.	

5.1.2 Read Cycle Timing Register-A (1F0h, Index-0, R/W)

This register shares the I/O address with the Read Cycle Timing Register-B, indexed by the Miscellaneous Register bit 0. It controls the read cycle timing of IDE data register for the drive selected by the Control register bits [3:2]. The bit field of this register is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	RDPW[3:0]	***Read Pulse Width:*** The value programmed in this register determines the DRD# pulse width in CLKs (for a 16-bit read from the IDE Data Register). See Table 5-6.	xxxx
[3:0]	RDREC[3:0]	***Read Recovery Time:*** The value programmed in this register determines the recovery time between the end of DRD# and the next DA[2:0]/DCSx# being presented (after a 16-bit read from the IDE Data Register), measured in CLKs. See Table 5-7.	xxxx

5.1.3 Read Cycle Timing Register-B (1F0h, Index-1, R/W)

This register shares the I/O address with the Read Cycle Timing Register-A, indexed by the Miscellaneous Register bit 0. It controls the read cycle timing of IDE data register for the drive not selected by the Control register bits [3:2], if the Control Register bit 7 is set The bit fields of these registers is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	RDPW[3:0]	***Read Pulse Width:*** The value programmed in this register determines the DRD# pulse width in CLKs (for a 16-bit read from the IDE Data Register). See Table 5-6.	xxxx
[3:0]	RDREC[3:0]	***Read Recovery Time:*** The value programmed in this register determines the recovery time between the end of DRD# and the next DA[2:0]/DCSx# being presented (after a 16-bit read from the IDE Data Register), measured in CLKs. See Table 5-7.	xxxx

5.1.4 Write Cycle Timing Register-A (1F1h, Index-0, R/W)

This register shares the I/O address with the Write Cycle Timing Register-B, indexed by the Miscellaneous Register bit 0. It controls the write cycle timing of IDE data register for the drive selected by the Control register bits [3:2]. The bit field of this register is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	WRPW[3:0]	***Write Pulse Width:*** The value programmed in this register determines the DWR# pulse width in CLKs (for a 16-bit write from the IDE Data Register). See Table 5-6.	xxxx
[3:0]	WRREC[3:0]	***Write Recovery Time:*** The value programmed in this register determines the recovery time between the end of DWR# and the next DA[2:0]/DCSx# being presented (after a 16-bit write from the IDE Data Register), measured in CLKs. See Table 5-7.	xxxx

5.1.5 Write Cycle Timing Register-B (1F1h, Index-1, R/W)

This register shares the I/O address with the Write Cycle Timing Register-A, indexed by the Miscellaneous Register bit 0. It controls the write cycle timing of IDE data register for the drive not selected by the Control register bits [3:2], if the Control Register bit 7 is set The bit fields of these registers is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	WRPW[3:0]	***Write Pulse Width:*** The value programmed in this register determines the DWR# pulse width in CLKs (for a 16-bit write from the IDE Data Register). SeeTable 5-6.	xxxx
[3:0]	WRREC[3:0]	***Write Recovery Time:*** The value programmed in this register determines the recovery time between the end of DWR# and the next DA[2:0]/DCSx# being presented (after a 16-bit write from the IDE Data Register), measured in CLKs. See Table 5-7.	xxxx

5.1.6 Control Register (1F3h, R/W)

Bits	Mnemonic	Description	Default
7	REGTIM2	***Enable Timing Registers-B.*** When set, this bit enables cycle-timing registers-B (1F0h & 1F1h of the Index-1) to override the IDE timing set by the strap options for any drive not selected by 1F3h bit [3:2]. It also enables the miscellaneous timing register 1F6h bits [5:1] to override the timing set by the strap options.	0
[6:5]	----	Reserved: Must always be written with '0'.	0
4	EN1WSRD	***Enable 1-Wait State Read.*** 1 = 1 WS minimum for data reads, 0 = 2 WS minimum.	0
3	REGTIM1	***Enable Timing Register-A, Drive 1:*** When set, this bit enables cycle-timing registers-A (1F0h & 1F1h of the Index-0) to override the IDE timing set by the strap options for Drive-1.	0
2	REGTIM0	***Enable Timing Register-A, Drive 0:*** When set, this bit enables cycle-timing registers-A (1F0h & 1F1h of the Index-0) to override the IDE timing set by the strap options for Drive-0.	0
1	ENSMI	***Enable SMI:*** When set, this bit generates an SMI upon access to any IDE I/O address, if ENDO is 1 and CNFDIS is 1. Clearing this bit will reset SMI and disables it.	0
0	----	Reserved - Must be written 1.	1

Note For all new software controls the IDE timing through registers programming, bits 2, 3 and 7 of the Control register should be enabled after the Cycle Timing Registers and Miscellaneous Register are programmed. See Table 5-1 for programming options.

5.1.7 Strap Register (1F5h)

Bits	Mnemonic	Description	Default
7	PCI3F7	***PCI 3F7 Read (Read/Write).*** Decides whether or not read access to 3F7h comes from local bus. 0 = 3F7h read from local bus. 1 = No response to 3F7h read.	
[6:5]	REV[1:0]	***Revision Number Register (Read Only).*** When the value of this register is set to 11, the content of REVID register should be used to find the revision level of the chip.	11
4	DINTR	***DINTR Status (Read Only).*** Returns the state of DINTR input.	
[3:2]	MODE[1:0]	***Mode (Read Only).*** Returns information about drive speed as determined by MODE[1:0] strap options. Please refer to the Mode Strap description for specific information.	
1	----	Reserved - Must be written 1.	
0	SPD0	***CLK Speed (Read/Write).*** PCI-Bus CLK frequency select. At reset time, the value of these bits is set by the sampling of SPD0 strap options. SPD0 CLK 0 33 MHz 1 25 MHz	

5.1.8 SMI Address Register (1F2h, Read Only)

Bits	Mnemonic	Description	Default
7	SMI	***SMI Status:*** This reflects the state of the SMI output from the PIC.	x
6	SMIW/R#	***SMI Last W/R#:*** The value of W/R# during the cycle that last caused an SMI.	x
5	SMIA9	***SMI Last A9:*** The value of HA9 during the cycle that last caused an SMI.	x
4	SMIA2	***SMI Last A2:*** The value of HA2 during the cycle that last caused an SMI.	x
[3:0]	SMIBE[3:0]	***SMI Last BEx#:*** The value of BE[3:0] during the cycle that last caused an SMI.	xxxx

5.1.9 SMI Data Register (1F4h, Read Only)

Bits	Mnemonic	Description	Default
[7:0]	SMIDATA	***SMI Data:*** If an 8-bit write cycle caused an SMI, this register returns the data written in that cycle.	xxxx xxxx

5.1.10 SMI Data Register (1F4h, Write Only))

Bits	Mnemonic	Description	Default
[7:4]	IRQTRAN	***IRQ14, IRQ15, INTA# Transition Bit:*** Writing a 1 to bit 7 allows IRQ14, IRQ15, and INTA# to transition from inactive to active during data read prefetch. Bits 6:4 are not used in write only mode.	xxxx xxxx
[3:0]	GPRI	***General Purpose Register Index:*** This is the index port for sixteen 8-bit registers located at data port 1F7h. Index Fh is reserved.	

5.1.11 Miscellaneous Register (1F6h, R/W)

Bits	Mnemonic	Description	Default
7	IDEFLOAT	***IDE Pins Float:*** When set, tri-states all the outputs and bi-directional pins connected to the IDE drive. (DRST#, DRD#, DWR#, DCS#3, DCS1#, DA[2:0] and DD[15:0])	0
6	ENPREF	***Enable Read Prefetch:*** Enables/Disables Read Prefetch. At reset time, the value of this register is set by ENPREF strap option. 1 = Enable, 0 = Disable.	
[5:4]	ASU[1:0]	***Address Setup Time:*** The value programmed in this register determines the address setup time between the DRD# or DWR# going active and the DA[2:0], DCS3#, DCS1# being presented, measured in CLKs. See Table 5-4.	x
[3:1]	DRDY[2:0]	***DRDY Delay:*** The value programmed in this register determines the minimum number of CLKs between DRDY# going high and DRD# or DWR# going inactive. See Table 5-5.	xx
0	INDEX-0	***Index-0:*** This bits is used to select between Cycle Timing Registers-A and -B located at 1F0h and 1F1h.	0

5.1.12 Index Data Register (1F7h, R/W)

Bits	Mnemonic	Description	Default
[7:0]	GPREG	***General Purpose Data Register:*** This is the data port for sixteen 8-bit registers indexed at data port 1F4h.	xxxx xxxx

5.2 I/O Registers for Secondary IDE

The register addresses are referred to in this section by their power-up default addresses. If the power-up default is modified by writing to configuration register IO3, then these registers will be relocated accordingly.

The PIC contains registers at seven I/O ports accessible after two consecutive 16-bit I/O reads from address 171h. Any other
I/O cycle between these two reads will disable access to the PIC registers.

5.2.1 Internal ID Register (172h, Write Only)

Bits	Mnemonic	Description	Default
7	CNFDIS	***Configuration Disable:*** This bit must be set to '0' in order to access 621A Internal Registers. Any write to this register with CNFDIS = 1 will disable all accesses to the 621A registers until another two consecutive I/O reads from 171h.	1
6	CNFOFF	***Configuration Off.*** This bit must be set to '0' in order to access 621A Internal Registers. Any write to this register with CNFOFF = 1 will disable all accesses to the 621A registers until power down or reset.	0
[5:2]	----	Reserved - Must be written 0.	
[1:0]	----	Reserved - Must be written 11.	

5.2.2 Read Cycle Timing Register-A (170h, Index-0, R/W)

This register shares the I/O address with the Read Cycle Timing Register-B, indexed by the Miscellaneous Register bit 0. It controls the read cycle timing of IDE data register for the drive selected by the Control register bits [3:2]. The bit field of this register is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	RDPW[3:0]	***Read Pulse Width:*** The value programmed in this register determines the DRD# pulse width in CLKs (for a 16-bit read from the IDE Data Register). See Table 5-6.	xxxx
[3:0]	RDREC[3:0]	***Read Recovery Time:*** The value programmed in this register determines the recovery time between the end of DRD# and the next DA[2:0]/DCSSx# being presented (after a 16-bit read from the IDE Data Register), measured in CLKs. See Table 5-7.	xxxx

5.2.3 Read Cycle Timing Register-B (170h, Index-1, R/W)

This register shares the I/O address with the Read Cycle Timing Register-A, indexed by the Miscellaneous Register bit 0. It controls the read cycle timing of IDE data register for the drive not selected by the Control register bits [3:2], if the Control Register bit 7 is set The bit fields of these registers is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	RDPW[3:0]	***Read Pulse Width:*** The value programmed in this register determines the DRD# pulse width in CLKs (for a 16-bit read from the IDE Data Register). See Table 5-6.	xxxx
[3:0]	RDREC[3:0]	***Read Recovery Time:*** The value programmed in this register determines the recovery time between the end of DRD# and the next DA[2:0]/DCSSx# being presented (after a 16-bit read from the IDE Data Register), measured in CLKs. See Table 5-7.	xxxx

5.2.4 Write Cycle Timing Register-A (171h, Index-0, R/W)

This register shares the I/O address with the Write Cycle Timing Register-B, indexed by the Miscellaneous Register bit 0. It controls the write cycle timing of IDE data register for the drive selected by the Control register bits [3:2]. The bit field of this register is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	WRPW[3:0]	***Write Pulse Width:*** The value programmed in this register determines the DWR# pulse width in CLKs (for a 16-bit write from the IDE Data Register). See Table 5-6.	xxxx
[3:0]	WRREC[3:0]	***Write Recovery Time:*** The value programmed in this register determines the recovery time between the end of DWR# and the next DA[2:0]/DCSSx# being presented (after a 16-bit write from the IDE Data Register), measured in CLKs. See Table 5-7.	xxxx

5.2.5 Write Cycle Timing Register-B (171h, Index-1, R/W)

This register shares the I/O address with the Write Cycle Timing Register-A, indexed by the Miscellaneous Register bit 0. It controls the write cycle timing of IDE data register for the drive not selected by the Control register bits [3:2], if the Control Register bit 7 is set The bit fields of these registers is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	WRPW[3:0]	***Write Pulse Width:*** The value programmed in this register determines the DWR# pulse width in CLKs (for a 16-bit write from the IDE Data Register). See Table 5-6.	xxxx

Bits	Mnemonic	Description	Default
[3:0]	WRREC[3:0]	***Write Recovery Time:*** The value programmed in this register determines the recovery time between the end of DWR# and the next DA[2:0]/DCSSx# being presented (after a 16-bit write from the IDE Data Register), measured in CLKs. See Table 5-7.	xxxx

5.2.6 Control Register (173h, R/W)

Bits	Mnemonic	Description	Default
7	REGTIM2	***Enable Timing Registers-B.*** When set, this bit enables cycle-timing registers-B (170h & 171h of the Index-1) to override the IDE timing set by the strap options for any drive not selected by 173h bit [3:2]. It also enables the miscellaneous timing register 176h bits [5:1] to override the timing set by the strap options.	0
[6:4]	----	Reserved: Must always be written with '0'.	0
3	REGTIM1	***Enable Timing Register-A, Drive 1:*** When set, this bit enables cycle-timing registers-A (170h & 171h of the Index-0) to override the IDE timing set by the strap options for Drive-1.	0
2	REGTIM0	***Enable Timing Register-A, Drive 0:*** When set, this bit enables cycle-timing registers-A (170h & 171h of the Index-0) to override the IDE timing set by the strap options for Drive-0.	0
1	ENSMI	***Enable SMI:*** When set, this bit generates an SMI upon access to any IDE I/O address, if ENDO is 1 and CNFDIS is 1. Clearing this bit will reset SMI and disables it.	0
0	----	Reserved - Must be written 1.	1

Note For all new software controls the IDE timing through registers programming, bits 2, 3 and 7 of the Control register should be enabled after the Cycle Timing Registers and Miscellaneous Register are programmed. See Table 5-1 for programming options.

5.2.7 Strap Register (175h)

Bits	Mnemonic	Description	Default
7	PCI3F7	***PCI 3F7 Read (Read/Write).*** Decides whether or not to respond to 3F7h read from local bus. 0 = 3F7h read from local bus. 1 = No response from 3F7h read.	
[6:5]	REV[1:0]	***Revision Number Register (Read Only).*** When the value of this register is set to 11, the content of REVID register should be used to find the revision level of the chip.	11
4	SDINTR	***SDINTR Status (Read Only).*** Returns the state of SDINTR input.	
[3:2]	----	Reserved - Must be written 0.	
1	----	Reserved - Must be written 1.	
0	----	Reserved - Must be written 0.	

5.2.8 SMI Address Register (172h, Read Only)

Bits	Mnemonic	Description	Default
7	SMI	***SMI Status:*** This reflects the state of the SMI output from the PIC.	x

Bits	Mnemonic	Description	Default
6	SMIW/R#	***SMI Last W/R#:*** The value of W/R# during the cycle that last caused an SMI.	x
5	SMIA9	***SMI Last A9:*** The value of HA9 during the cycle that last caused an SMI.	x
4	SMIA2	***SMI Last A2:*** The value of HA2 during the cycle that last caused an SMI.	x
[3:0]	SMIBE[3:0]	***SMI Last BEx#:*** The value of BE[3:0] during the cycle that last caused an SMI.	xxxx

5.2.9 SMI Data Register (174h, Read Only)

Bits	Mnemonic	Description	Default
[7:0]	SMIDATA	***SMI Data:*** If an 8-bit write cycle caused an SMI, this register returns the data written in that cycle.	xxxx xxxx

5.2.10 Miscellaneous Register (176h, R/W)

Bits	Mnemonic	Description	Default
7	----	Reserved - Must be written 0.	0
6	ENPREF	***Enable Read Prefetch:*** Enables/Disables Read Prefetch. At reset time, the value of this register is set by ENPREF strap option. 1 = Enable, 0 = Disable.	
[5:4]	ASU[1:0]	***Address Setup Time:*** The value programmed in this register determines the address setup time between the DRD# or DWR# going active and the DA[2:0], DCSS3#, DCSS1# being presented, measured in CLKs. See Table 5-4.	x
[3:1]	DRDY[2:0]	***DRDY Delay:*** The value programmed in this register determines the minimum number of CLKs between DRDY# going high and DRD# or DWR# going inactive. See Table 5-5.	xx
0	INDEX-0	***Index-0:*** This bits is used to select between Cycle Timing Registers-A and -B located at 170h and 171h.	0

5.3 Programming the IDE Controller Registers

The following steps describe how to program the 82C621A index registers to support different IDE modes. The chip should be booted at 50MHz, mode 0 (from strapping), before you program different modes.

1. Program proper values into 1F0h and 1F1h, they are the default for Timing Register-A.
2. Set bit 0 of 1F6h to 1 to switch to Timing Register-B.
3. Program proper values into 1F0h and 1F1h, they reflect Timing Register-B.
4. Program proper values into bits [5:1] of 1F6h. It affects both Timing Register-A and Timing Register-B.
5. Enable bits 2, 3 and 7 in 1F3h. The following table describes the options for programming these three bits:

Table 5-1 REGTIMx Programming Options

REGTIM0	REGTIM1	REGTIM2	Drive 0 Control	Drive 1 Control
1*	0	1	Index-0	Index-1
0	1	1	Index-1	Index-0
0	0	1	Index-1	Index-1
1	0	0	Index-0	Straps
0	1	0	Straps	Index-0
0	0	0	Straps	Straps
1	1	x	Index-0	Index-0

*. Recommended Configuration

The following tables show the recommended index register clock settings to interface to different modes of the IDE drives.

Table 5-2 16-Bit Timing (LCLKs)

	PCI Bus Frequency							
	25MHz, 40ns				33MHz, 30ns			
Mode	0	1	2	3	0	1	2	3
Address Setup	2	2	1	1	3	2	2	1
Command Pulse	5	4	3	2	6	5	4	3
Recovery Time	8	4	2	2	11	6	2	2
DRDY	2	2	2	2	2	2	2	2

Table 5-3 8-Bit Timing (LCLKs)

	PCI Bus Frequency							
	25MHz, 40ns				33MHz, 30ns			
Mode	0	1	2	3	0	1	2	3
Address Setup	2	2	1	1	3	2	2	1
Command Pulse	9	9	9	9	11	11	11	11
Recovery Time	8	8	8	8	11	11	11	11
DRDY	5	5	5	5	6	6	6	6

Note The 8-bit settings are fixed and cannot be programmed.

Table 5-4 Address Setup

Bit 5	Bit 4	Timing, in LCLKs
0	0	1
0	1	2
1	0	3
1	1	4

Note Index Registers 1F6h/176h bits [5:4]

Table 5-5 DRDY Delay

Bit 3	Bit 2	Bit 1	Timing, in LCLKs
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	7
1	1	0	8
1	1	1	9

Note Index Registers 1F6h/176h bits [3:1]

Table 5-6 Read/Write Command Pulse

Bit 7	Bit 6	Bit 5	Bit 4	Timing, in LCLKs	
				Read Command 1F0h/170h	Write Command 1F1h/171h
0	0	0	0	1	1
0	0	0	1	2	2
0	0	1	0	3	3
0	0	1	1	4	4

Bit 7	Bit 6	Bit 5	Bit 4	Timing, in LCLKs	
				Read Command 1F0h/170h	Write Command 1F1h/171h
0	1	0	0	5	5
0	1	0	1	6	6
0	1	1	0	7	7
0	1	1	1	8	8
1	0	0	0	9	9
1	0	0	1	10	10
1	0	1	0	11	11
1	0	1	1	12	12
1	1	0	0	13	13
1	1	0	1	14	14
1	1	1	0	15	15
1	1	1	1	16	16

Note Index Registers 1F0h/170h (Read) or 1F1h/171h (Write), Index 0/1, bits [7:4]

Table 5-7 Read/Write Recovery Time

Bit 3	Bit 2	Bit 1	Bit 0	Timing, in LCLKs	
				Read Recovery 1F0h/170h	Write Recovery 1F1h/171h
0	0	0	0	2	2
0	0	0	1	3	3
0	0	1	0	4	4
0	0	1	1	5	5
0	1	0	0	6	6
0	1	0	1	7	7
0	1	1	0	8	8
0	1	1	1	9	9
1	0	0	0	10	10
1	0	0	1	11	11
1	0	1	0	12	12
1	0	1	1	13	13
1	1	0	0	14	14
1	1	0	1	15	15
1	1	1	0	16	16
1	1	1	1	17	17

Note Index Registers 1F0h/170h (Read) or 1F1h/171h (Write) Index 0/1, bits [3:0]

6.0 AC Characteristics

Temperature: 0°C to 70°C, Vcc: 5V ± 5%, 50pF load

Sym.	Description	Min (ns)	Typ (ns)	Max (ns)
t1	FRAME#, IRDY#, AD[31:0], PAR, C/BE[3:0]#, IDSEL setup time to CLK ↑	7.0		
t2	FRAME#, IRDY#, AD[31:0], PAR, C/BE[3:0]#, IDSEL hold time to CLK ↑	0.0		
t3	CLK ↑ to DEVSEL#, TRDY#, STOP#, PERR# valid	1.0		11.0
t4	CLK ↑ to DEVSEL#, TRDY#, STOP#, PERR# invalid	1.0		11.0
t5	CLK ↑ to DEVSEL#, TRDY#, STOP#, PERR# float	1.0		11.0
t6	CLK ↑ to AD[31:0], PAR valid (continuous data stepping)	2.0		25.0
t7	CLK ↑ to AD[31:0] float	2.0		25.0
t8	CLK ↓ to AD[31:0] valid (1-WS read: continuous data stepping)	3.0		25.0
t9	CLK ↑ to DRD#, DWR#, DA[2:0], DCS3#, DCS1#, DCSS3#, DCSS1#, ROMCS# valid	2.0		30.0
t10	CLK ↑ to DRD#, DWR#, DA[2:0], DCS3#, DCS1#, DCSS3#, DCSS1#, ROMCS# invalid	2.0		30.0
t11	CLK ↑ to DD[15:0] valid	2.0		
t12	CLK ↑ to DD[15:0] float	1.0		30.0
t13	CLK ↑ to ADLE valid	1.0		20.0
t14	DSKCHNG# active to AD[31:0] valid	1.0	9.0	30.0
t15	CLK ↑ to CHRDY# valid	3.0	9.0	20.0
t16	CLK ↑ to CHRDY# float	3.0	9.0	20.0
t17	CLK ↑ to SMI active	3.0	14.0	40.0
t18	CLK ↑ to RD3F7# active	6.0	17.0	33.0
t19	IORC# active to RD3F7# active	2.0	10.0	33.0
t20	IORC# inactive to RD3F7# inactive	2.0	10.0	33.0
t21	RST# active to DRST# active delay	2.0	10.0	20.0

6.1 Absolute Maximum Ratings

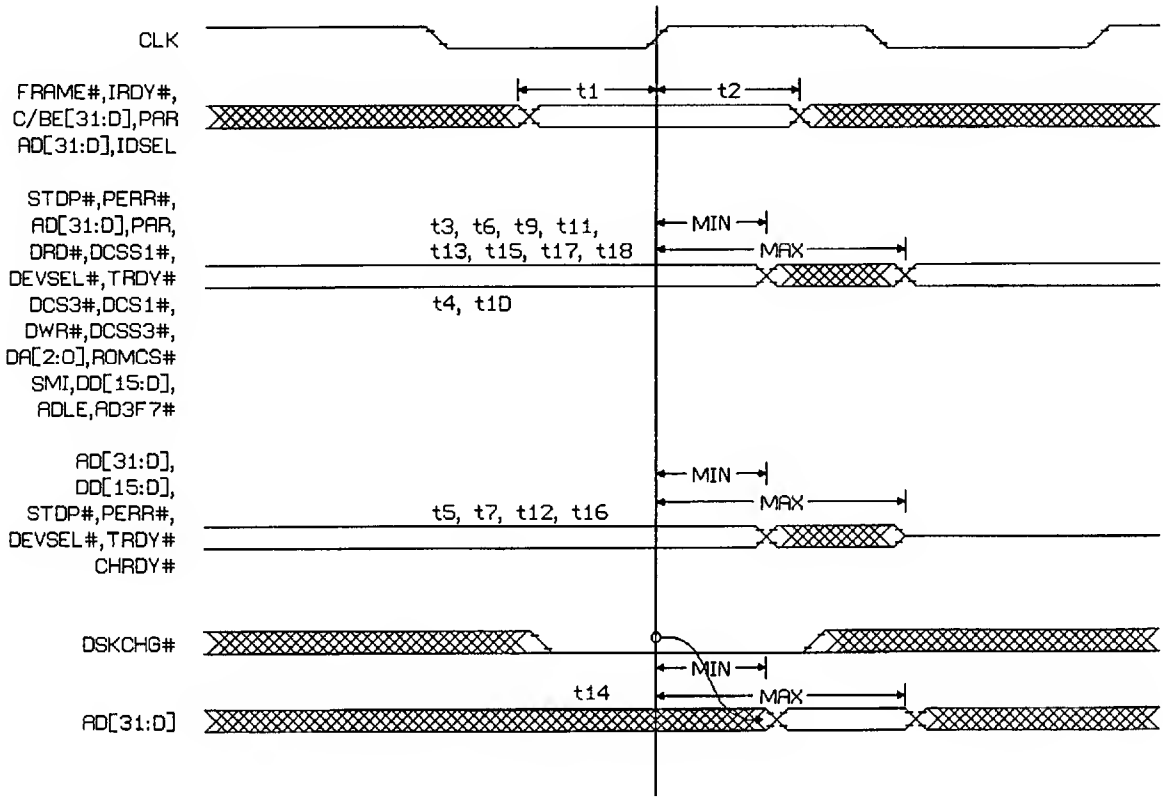
Sym	Description	Min	Max	Units
V_{CC}	Supply Voltage		6.5	V
V_I	Input Voltage	-0.5	5.5	V
V_O	Output Voltage	-0.5	5.5	V
T_{OP}	Operating Temperature	-25	70	°C
T_{STG}	Storage Temperature	-40	125	°C

6.2 DC Characteristics

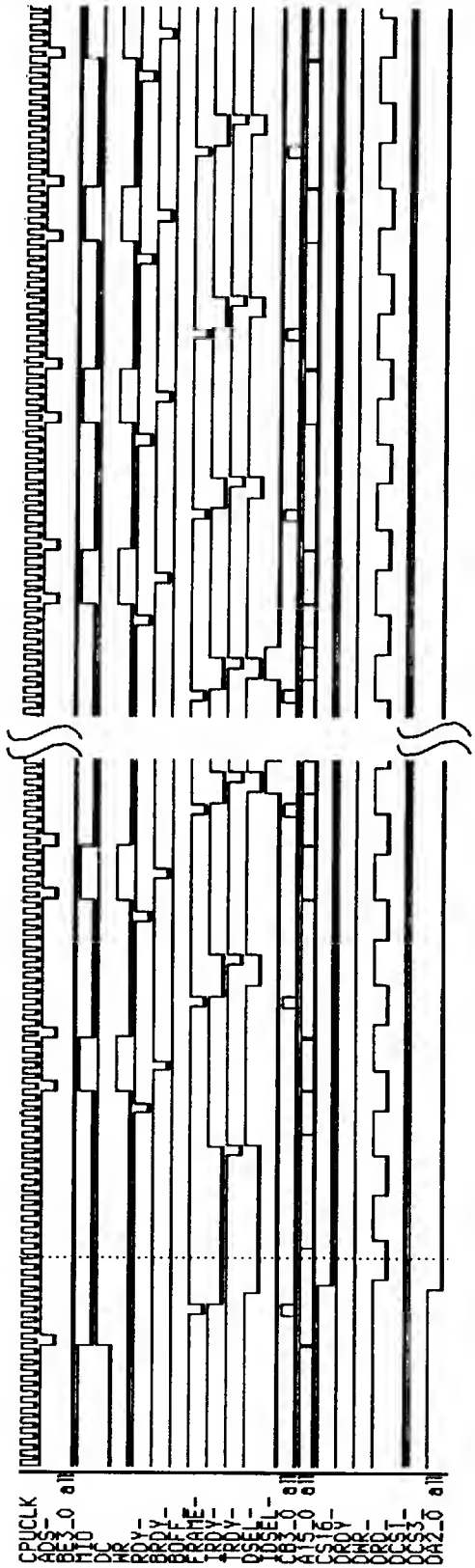
Sym	Description	Min	Max	Units
VIL1	Input Low Voltage for SPD0, ISA3F7, ENPREF, MODE[1:0], RELOC, FNC0, INTLEV, TOMD#		1.35	V
VIH1	Input High Voltage for SPD0, ISA3F7, ENPREF, MODE[1:0], RELOC, FNC0, INTLEV, TOMD#	3.85		V
VIL2	Input Low Voltage for all other pins		.08	V
VIH2	Input High Voltage for all other pins	2.0		V
VOL	Output Low Voltage 4mA for AD[31:0], INTA#, RD3F7#, ROMCS#/SMI, ADLE, INTB#, PAR 6mA for DEVSEL#, TRDY#, STOP#, PERR# 16mA for CHRDY#, DRST#, DA[2:0], DD[15:0], DRD#, DWR#, DCS1#, DCS3#, DCSS1#, DCSS3#		0.5	V
VOH	Output High Voltage 4mA for AD[31:0], RD3F7#, ROMCS#/SMI, ADLE, PAR 6mA for DEVSEL#, TRDY#, STOP#, PERR# 16mA for DRST#, DA[2:0], DD[15:0], DRD#, DWR#, DCS1#, DCS3#, DCSS1#, DCSS3#	2.4		V
IIL	Input Leakage Current (VIN = VCC)		10	uA
IOZ	Tri-state Leakage Current		10	uA
CIN	Input Capacitance		10	pF
COUT	Output Capacitance		10	pF
CIO	I/O Capacitance		12	pF
ICC	Power Supply Current		TBA	mA
ICCS	Power Supply Current, Standby		TBA	mA

6.3 Timing Waveforms

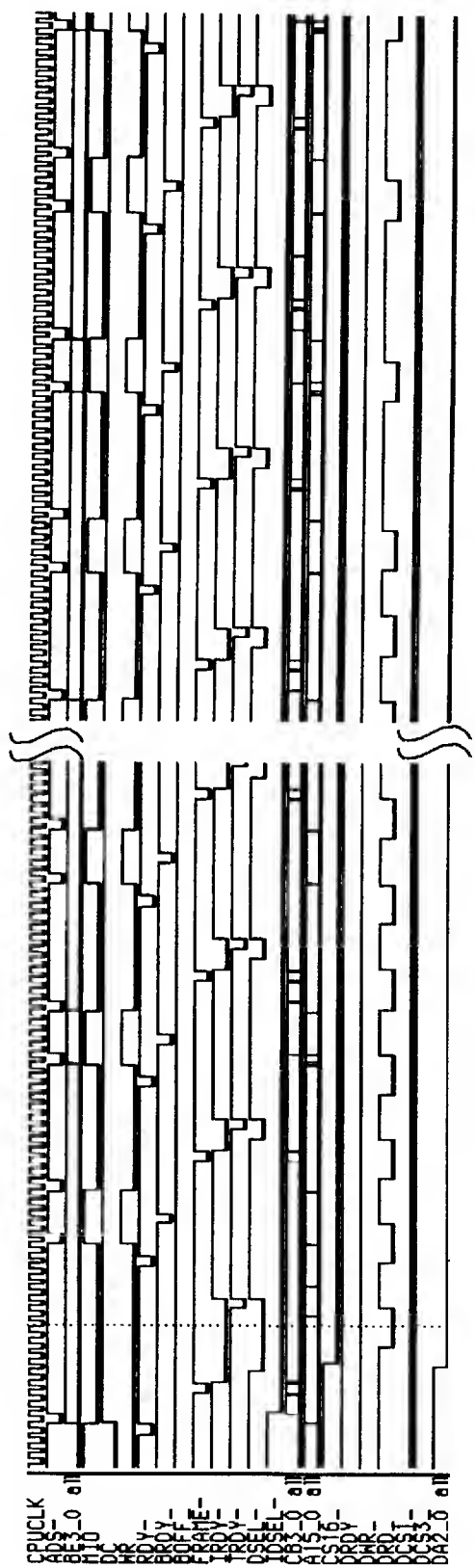
6.3.1 Input and Output Waveform



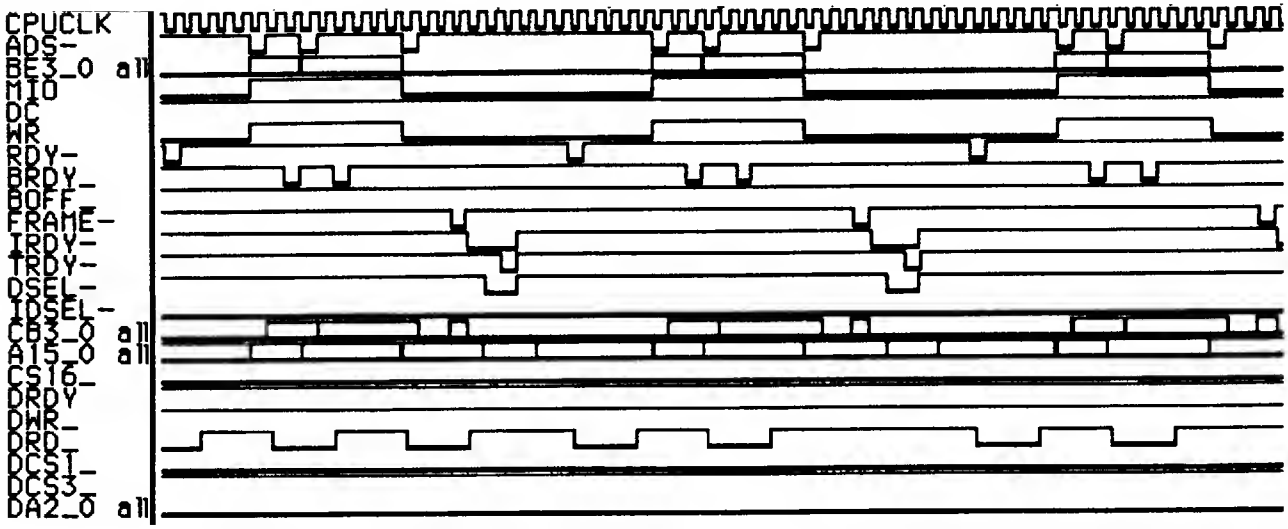
6.3.2 32-Bit I/O Access - Read Prefetch Enabled



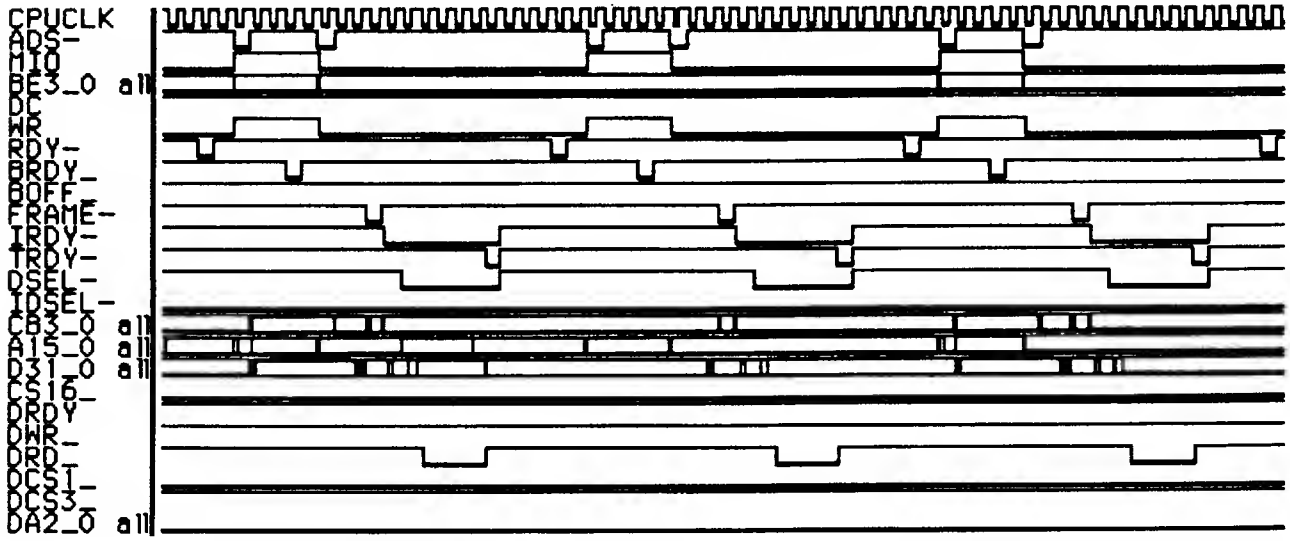
6.3.3 16-Bit I/O Access - Read Prefetch Enabled



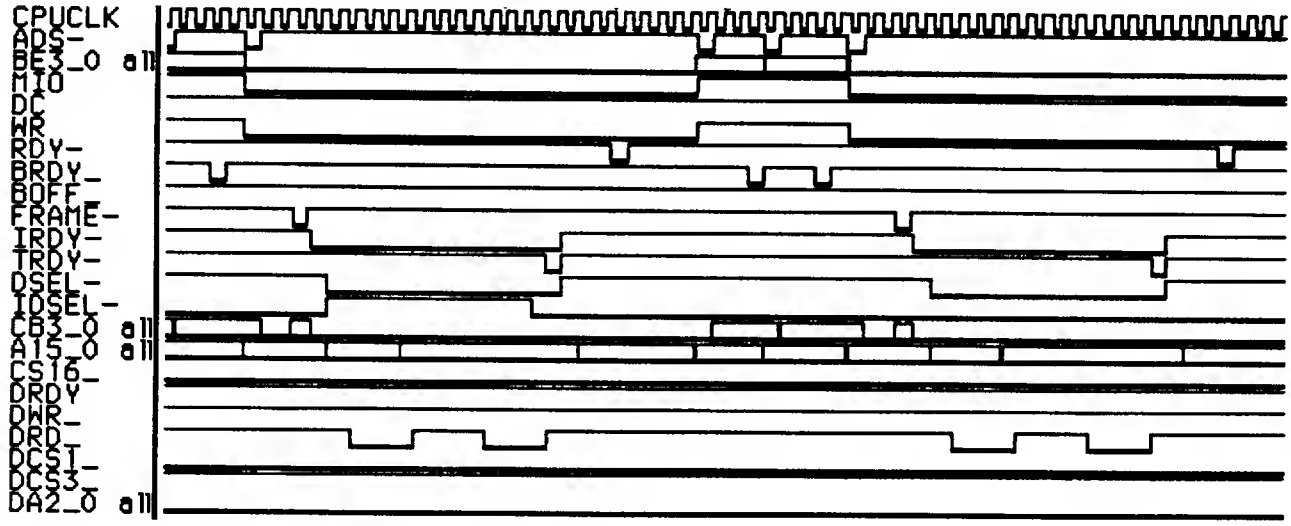
6.3.4 32-Bit I/O Access -Buffer Full



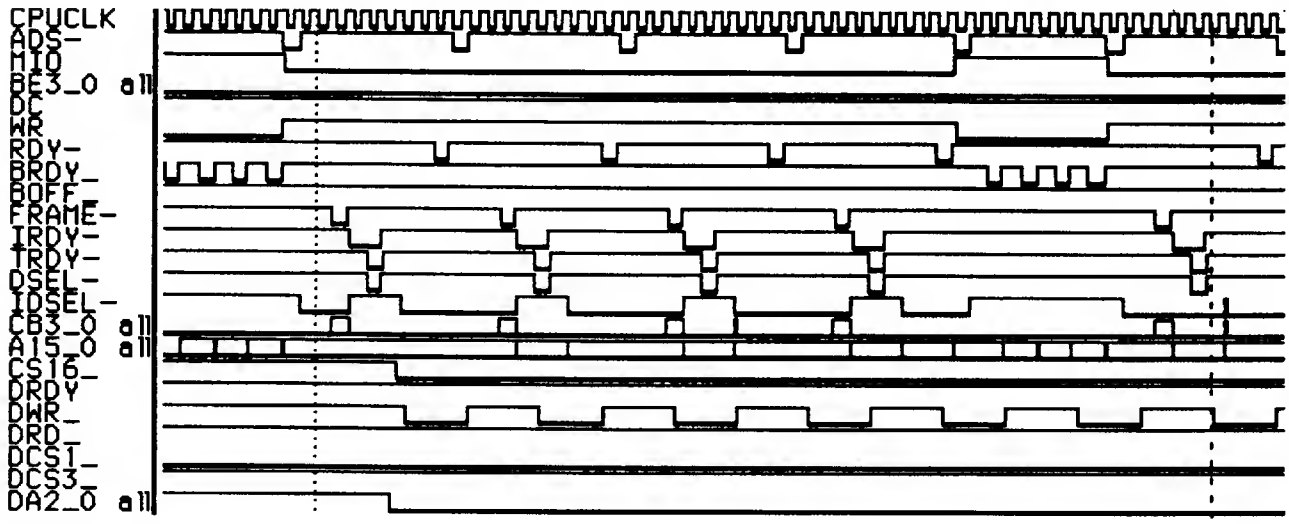
6.3.5 16-Bit I/O Access - No Prefetch



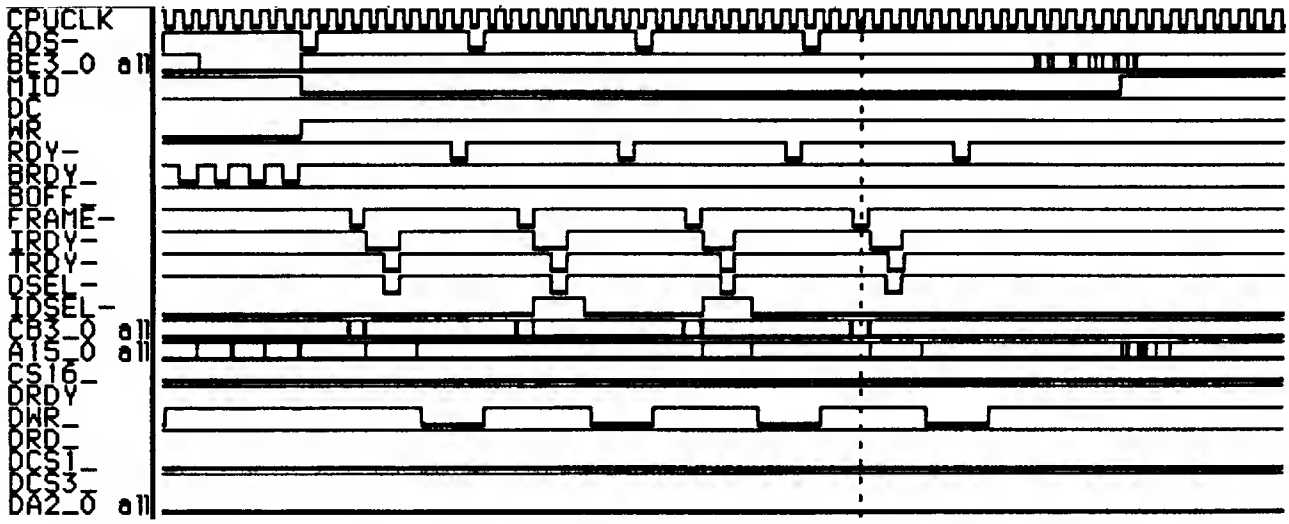
6.3.6 32-Bit I/O Access - No Prefetch



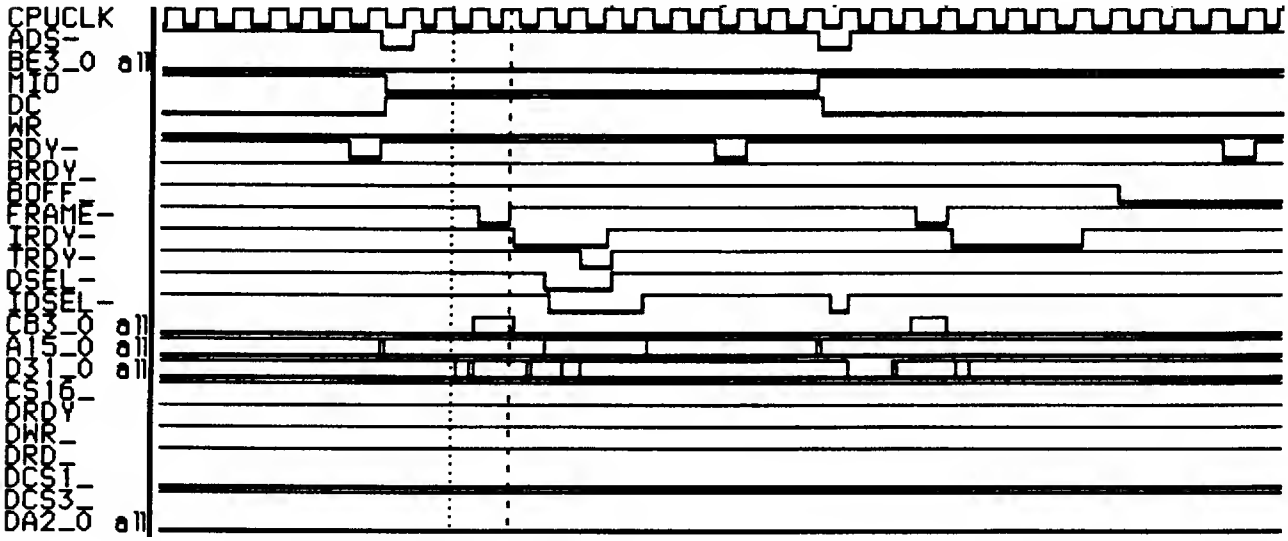
6.3.7 32-Bit I/O Write



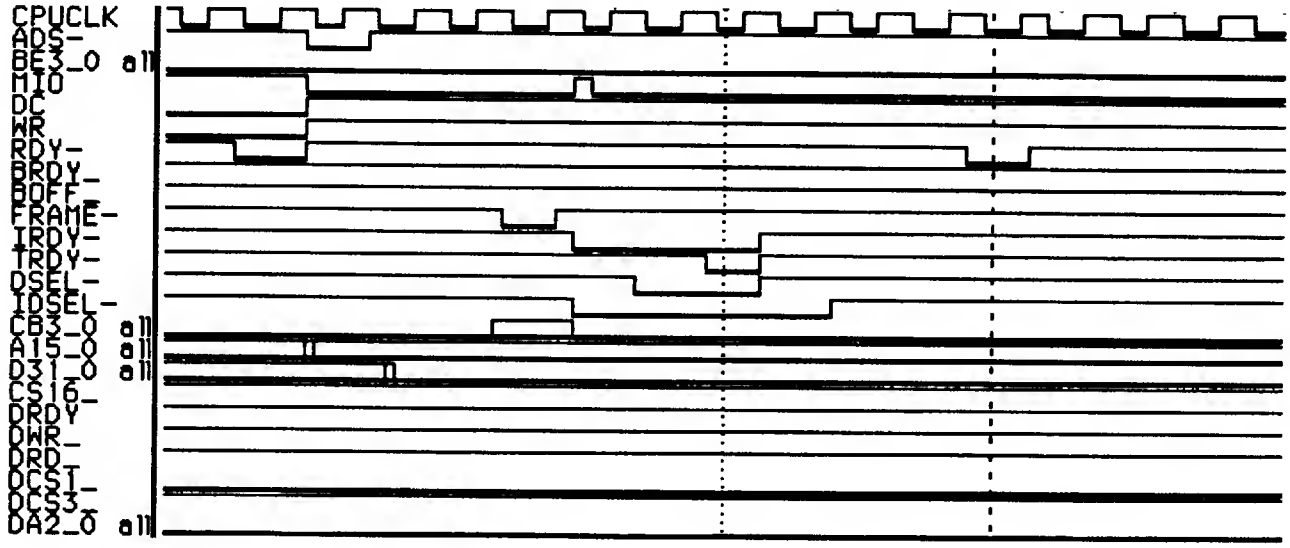
6.3.8 16-Bit I/O Write



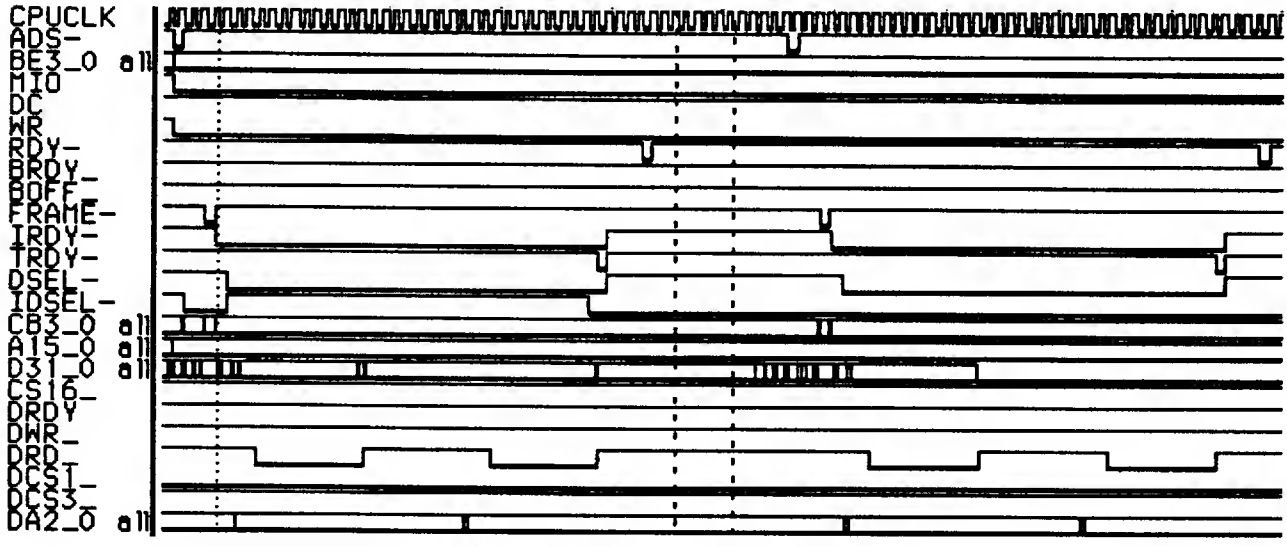
6.3.9 PCI Configuration Read Cycle



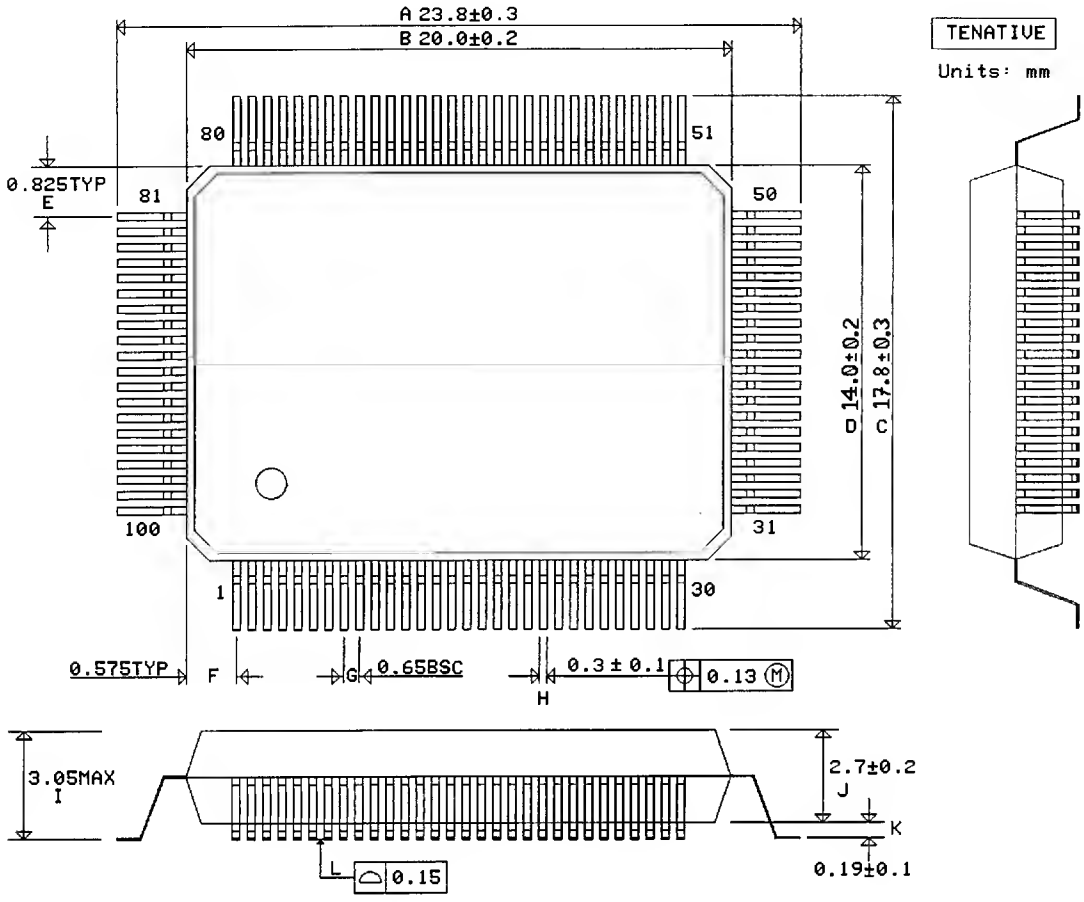
6.3.10 PCI Configuration Write Cycle

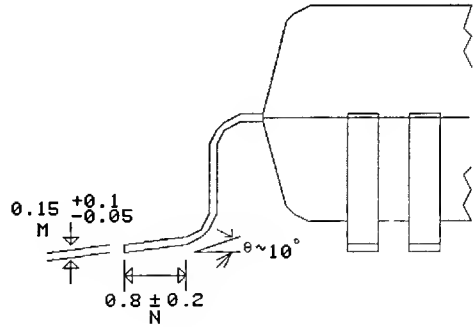


6.3.11 Enter 611 Register Programming Mode (Read 1F1h twice)



7.0 Mechanical Package





DIM	MILLIMETERS		INCHES		DESCRIPTION
	MIN	MAX	MIN	MAX	
A	23.5	24.1	.925"	.949"	Maximum Width LEAD TO LEAD
B	19.8	20.2	.779"	.795"	Maximum Width PACKAGE ENVELOPE
C	17.5	18.1	.689"	.713"	Maximum Height LEAD TO LEAD
D	13.8	14.2	.543"	.559"	Maximum Height PACKAGE ENVELOPE
E	0.825 TYP		.0325" TYP		LEAD CENTER TO PERP. LEAD PLANE
F	0.575 TYP		.0226" TYP		LEAD CENTER TO PERP. LEAD PLANE
G	0.65 BSC		.0256" BSC		LEAD TO LEAD CENTER SPACING
H	0.2	0.4	.008"	.016"	LEAD WIDTH
I	——	3.05	——	.120"	PACKAGE HEIGHT LEAD PLANE TO TOP
J	2.5	2.9	.098"	.114"	MAXIMUM THICKNESS PACKAGE ENVELOPE
K	0.09	0.29	.0035"	.0114"	LEAD PLANE TO PACKAGE BOTTOM
L	——	0.15	——	.006"	LEAD PLANE SKEW
M	0.1	0.25	.004"	.010"	LEAD THICKNESS
N	0.6	1.0	.024"	.039"	LEAD FOOTPRINT